a second bias transistor having a current path from the second end of said resistor to the voltage reference, and having a control element connected to the second end of said resistor and to the first end of the current path of said second input transistor;

a capacitor having a first plate and having a second plate connected to the voltage reference;

an output stage having an input connected to the first plate of said capacitor and having an output;

a programmable delay control circuit having a plurality of enable outputs;

a plurality of constant-current sources, each constant current source of the plurality of constant-current sources having a current path between a corresponding enable output of said programmable delay control circuit and the first plate of said capacitor, and having a bias input connected to the control element of said first bias transistor such that the current flowing in the first bias transistor is proportionately mirrored in the current path of each constant-current source of the plurality of constant-current sources, responsive to the corresponding enable output and wherein a constant of proportionality may be chosen independently of the constant of proportionality of any other constant-current source; and

a plurality of constant-current drains, each constant current drain of the plurality of constant-current drains having a current path between the corresponding enable output of said programmable delay control circuit and the first plate of said capacitor, and having a bias input connected to the control element of said second bias transistor such that the current flowing in the second bias transistor is proportionately mirrored in the current path of each constant-current drain of the plurality of constant-current drains, responsive to the corresponding enable output and wherein a constant of proportionality may be chosen independently of the constant of proportionality of any other constant-current drain.

8. The delay circuit of claim 7 wherein said programmable delay control circuit comprises a digital circuit.

9. The delay circuit of claim 8 wherein the digital circuit comprises programmable memory circuit.

10. The delay circuit of claim 9 wherein the programmable memory circuit comprises a programmable read only memory.

11. The delay circuit of claim 10 wherein the programmable read only memory comprises a EEPROM.

12. The delay circuit of claim 9 wherein the programmable memory circuit comprises a FLASH memory.

13. A delay circuit comprising:

a plurality of current mirror current elements, with each current mirror current element having an enable input, having an input for receiving an input signal and having a constant current output for providing a constant current responsive to the input signal;

a programmable delay control circuit having a plurality of enable signals, each enable signal connected to the plurality of current mirror current elements so as to selectively enable a current mirror current element of the plurality of current mirror current elements;

a fixed capacitor having a first plate and a second plate, the first plate of the capacitor connected to the constant current outputs of the plurality of current mirror current elements, the second plate connected to a voltage reference, with each current mirror current element having a current path between a corresponding enable signal of said programmable delay control circuit and the first plate of said capacitor; and

an output stage having an input connected to the first plate of the capacitor and having an output for providing an output responsive to the voltage on the capacitor,

wherein a delay on an active edge of the input signal is adjustable by the programmable delay control circuit selectively enabling the enable signal of one or more of the plurality of current mirror current elements to change an overall current provided by the plurality of current mirror current elements to the first plate of the capacitor.

14. The delay circuit of claim 13, wherein the active edge of the input signal is a rising edge of the input signal and the plurality of current mirror current elements are a plurality of current mirror current sources, and a delay on the rising edge of the input signal is adjustable by the programmable delay control circuit selectively enabling the enable signal of one or more of the plurality of current mirror current sources to change an overall current source current provided by the plurality of current mirror current sources to the first plate of the capacitor.

15. The delay circuit of claim 13, wherein the active edge of the input signal is a falling edge of the input signal and the plurality of current mirror current elements are a plurality of current mirror current drains, and a delay on the falling edge of the input signal is adjustable by the programmable delay control circuit selectively enabling the enable signal of one or more of the plurality of current mirror current drains to change an overall current drain current provided by the plurality of current mirror current drains to the first plate of the capacitor.

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